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Resolving microscopic interfaces in Si$_{1-x}$Ge$_x$ alloy nanowire devices

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Abstract
We have fabricated Si$_{1-x}$Ge$_x$ alloy nanowire devices with Ni and Ni/Au electrodes. The electrical transport characteristics of the alloy nanowires depended strongly on the annealing temperature and contact metals. Ni/Au-contacted devices annealed at 400 $^\circ$C showed p-type transistor behavior as well as a resistance switching effect, while no switching was observed from Ni-contacted alloy nanowire devices. To identify the origin of such a hysteretic resistance switching effect, we constructed nanowire devices on a 40 nm Si$_3$N$_4$ membrane. Transmission electron microscopy analysis combined with electrical transport measurements revealed that devices contacted with Ni/Au, and thereby showing resistance switching, have Au atoms right next to the alloy nanowire.

Supplementary data are available from stacks.iop.org/Nano/20/115708

Some figures in this article are in colour only in the electronic version

1. Introduction

The interfaces between metals and semiconductors play a crucial role in determining the electronic properties of semiconductors, and hence the device performances. Numerous studies have sought to resolve the phenomena that occur at such interfaces using various techniques, including high-resolution transmission electron microscopy (HRTEM) [1], ballistic electron emission microscopy (BEEM) [2], Rutherford backscattering spectroscopy [3] and Auger electron spectroscopy [4]. However, most such analyses have been performed on bulk materials: the interfaces between metals and semiconductor nanostructures have yet to be resolved. Among other nanostructures, semiconducting nanowires have potential uses in diverse applications. Electronic and optoelectronic devices such as field effect transistors [5], switching memory [6], light emitting diodes [7], photosensors [8], and chemical [9] and biological sensors [10] have been successfully demonstrated using semiconductor nanowires; energy-storing or harvesting devices based on nanowires [11] have also recently been reported.

Several issues remain to be addressed, however, for the successful implementation of nanowires in electronic building blocks, including gaining control over the structural and physical properties of nanowires, and establishing good contact between the electrodes and the nanowires. To achieve such a control over nanowire devices, it is important to understand the nature of nanowires and contacts to nanowires. With recent advances in analytical technology, it is possible to observe a single Au atom impurity in a Si nanowire. For example, Allen et al identified the presence of Au catalyst atoms in Si nanowires using scanning transmission electron microscopy (STEM) [12], while de Hertog et al observed and controlled the diffusion of Au catalyst atoms on the surface of Si nanowires [13].

In this report, we show that Si$_{1-x}$Ge$_x$ alloy nanowires with Ni/Au contacts annealed at 400 $^\circ$C exhibit bias-dependent resistance switching behavior, and that this anomalous phenomenon stems from diffused Au atoms at the interface between the contact electrodes and the alloy nanowire.
2. Experimental details

Single-crystalline alloy nanowires with sub-100 nm diameters and lengths up to several microns were grown vertically on silicon substrates by the vapor–liquid–solid (VLS) method. Briefly, single-crystalline Si$_{1-x}$Ge$_x$ alloy nanowires ($x = 0.05–0.3$) were synthesized using Au catalyst deposited Si(111) substrates in a silicon tetrachloride (SiCl$_4$) based horizontal hot-wall chemical vapor transport system. The substrates were inserted into the center of a quartz tube and solid metallic Ge (purity 99.99%) powder was placed 1 inch away from the substrates as the Ge source. The temperature of the furnace was increased at a rate of 50 °C min$^{-1}$ to 1000 °C under a flow of H$_2$ and Ar at a rate of 100 sccm. Simultaneously, SiCl$_4$ as the Si source was introduced into the tube using H$_2$ carrier gas that was bubbled through the liquid source held at 0 °C at a flow rate of 20 sccm for 30 min. Then, the samples were allowed to cool down to room temperature under a H$_2$ and Ar atmosphere [14]. Nanowires collected from the substrates were dispersed in ethanol, and individual Si$_{1-x}$Ge$_x$ nanowires were placed on a heavily doped Si substrate with a 500 nm thick SiO$_2$ surface layer; a heavily doped Si substrate was used as a back gate. Patterns for the electrical wires were generated using an electron-beam lithography system. Before contact formation, the outer oxide layer of the Si$_{1-x}$Ge$_x$ alloy nanowires was etched using a 3% HF solution for 3–20 s. Then, 150 nm of Ni and 50 nm of Au were deposited successively on the contact area by electron-beam evaporation, followed by a gentle lift-off process. To form stable electrical contacts between the Si$_{1-x}$Ge$_x$ alloy nanowire and Ni/Au electrodes, we annealed the samples at 300 °C for 10 min in an Ar atmosphere or at 400 °C for 30 s using rapid thermal annealing (RTA).

To perform HRTEM analysis on nanowire devices, it is necessary to construct devices on transparent Si$_3$N$_4$ membranes. First, patterns for the transparent membrane were made with photolithography on the backside of Si(100) wafers with 40 nm thick Si$_3$N$_4$ and 200 nm thick SiO$_2$. Then, a dry etch (SF$_6$) was used to remove the Si$_3$N$_4$, followed by wet etching of SiO$_2$ and Si. After the membrane formation, device fabrication procedure is the same as for devices on SiO$_2$/Si substrates. TEM analyses were performed at National NanoFab Center, using a JEOL JEM-2100F microscope. We used 200 keV as the acceleration voltage.

3. Results and discussion

Figure 1 shows the electrical transport measured from Si$_{1-x}$Ge$_x$ alloy nanowire devices with Ni/Au contact electrodes. This particular device was fabricated on a SiO$_2$/Si substrate and annealed at 400 °C. The inset shows an SEM image of the device.

Figure 1. Bias-dependent resistance switching in a Si$_{95}$Ge$_{5}$ alloy nanowire device with Ni/Au contact electrodes. This particular device was fabricated on a SiO$_2$/Si substrate and annealed at 400 °C. The inset shows an SEM image of the device.

and the Si$_{1-x}$Ge$_x$ alloy. Interfacial interactions with various metals (e.g., Ni, Pt, Pd, Ti, and Co) have been investigated previously. For example, nickel silicide is a good candidate because of its low resistivity and thermal budget [16]. After the pioneering work of Wu et al., which showed the possibility of silicide contact in nanowire devices [17], Appenzeller et al. [18] and Weber et al. [19] demonstrated that a nickel silicide contact can be used to achieve stable contact between a Si nanowire and a metal electrode, and that the active channel length of the nanowire can be controlled by controlling the depth of the nickel silicide layer.

Before annealing, Si$_{1-x}$Ge$_x$ alloy nanowires showed very high resistance and a poor gate effect (supporting information, figure S1 available at stacks.iop.org/Nano/20/115708); however, after RTA at 400 °C, the current measured from the device increased by more than two orders of magnitude, and clear p-type transport behavior was observed, as reported in our previous publication [14]. As observed by others [18, 19], however, the electrical characteristics of Ni-contacted nanowires depend heavily on the annealing temperature. When annealed at a higher temperature of 500 °C, the nanowire exhibits metallic conductance, as shown in the supporting information figure S2 (available at stacks.iop.org/Nano/20/115708). Such metallic conductance in the nanowire can be explained by the fact that the entire Si$_{1-x}$Ge$_x$ alloy nanowire changed into a metallic silicide nanowire by axial diffusion of nickel into the nanowire.

As shown in figure 1, the device becomes highly conducting (ON) by ramping the bias voltage up to 2 V. The conductance decreases abruptly at around 0.2 V (RESET) when the sweep direction is reversed. Similar behavior is observed in the reverse bias region, although the RESET voltage is not as sharp in this region. The resistance switching effect also depends on the sweep speed, as shown in the supporting information (figure S3 (available at stacks.iop.org/Nano/20/115708)). Hysteresis increases with
between Au catalyst and nanowire is abrupt in VLS-grown
placement, (b) electrode fabrication, (c) annealing at 400 ◦C, and (d) side view of the device.

reduced sweep speed. The on/off ratio of the device ramped at
0.14 V s−1 is about 15, while the on/off ratio with a 0.7 V s−1
sweep is about 12. Such behavior suggests the presence of a
slow charge trap in the nanowire. Unlike some organic-
molecule-based memories, no negative differential resistance
(NDR) was observed, even at higher bias voltages. Most of the
Ni/Au-contacted Si1−xGex alloy nanowire devices fabricated
in the present study showed symmetric current-controlled S-
shaped current–voltage (I–V) curves similar to those shown in
figure 1. The switching behaviors in 400 ◦C annealed, Ni/Au-
contacted Si1−xGex alloy nanowire devices are universal,
regardless of the Ge content. The resistance switching effects
measured for Si70Ge30 and Si85Ge15 nanowire devices are
shown in the supporting information (figure S4 (available at
stacks.iop.org/Nano/20/115708)).

To investigate the origin of the resistance switching effect
in Si1−xGex alloy nanowire devices, it is important to analyze
the nanowire devices using high-resolution transmission
electron microscopy (HRTEM) with energy-dispersive x-ray
spectroscopy (EDX). To obtain TEM images of nanowire
deVICES, it is necessary to construct the devices on a transparent
membrane. Therefore, we constructed nanowire devices on
40 nm thick Si3N4 membranes, as shown in scheme 1. The
pattern generation, metalization, and annealing conditions are
the same as for the devices fabricated on SiO2/Si. Figure 2
shows TEM images of the Ni/Au-contacted Si85Ge5 alloy
nanowire devices and energy-dispersive x-ray analysis (EDS)
undertaken at different positions along a nanowire device.

The most striking observation here is that along with the
nickel germanosilicide we expected to find, we observed
Au-rich regions at the contact front: the border between
the alloy nanowire and the nickel silicide (red arrow in
figure 2(b)). The interfaces between the Au-rich domains
and crystalline alloy nanowires are atomically sharp, and
parallel to the Si1−xGex(110) plane. It is interesting to
compare this with the PtSi/Si interface, which also showed
an atomically sharp interface [20]. Also, the interface
between Au catalyst and nanowire is abrupt in VLS-grown
nanowires. The EDS line profile in figure S5 (available at
stacks.iop.org/Nano/20/115708) also shows clearly enhanced
Au concentrations at the contact front. Since Ni can form
NiSi below 350 ◦C, and the eutectic temperature of Au with
Si is around 359 ◦C, we may expect that we have complex
alloys at our annealing condition (400 ◦C). Ni/Au is a favored
pair for ohmic contacts for p-GaN or Schottky contacts for n-
GaN, since new Ni4N and AuGa2 compounds can form at the
interface by relatively low-temperature annealing [1]. It is well
known that Au can penetrate Ni films when annealed at 350 ◦C
for 10 min, and Hu et al reported layer reversal of Au and Ni
layers for samples annealed above 450 ◦C [3]. In this regard,
we may interpret the Au-rich regions at the contact front as an
AuSi alloy formed by an inter-diffused Au layer from the top.

Figure 3 shows the I–V characteristics of Ni/Au-
contacted Si85Ge5 (the same one in figure 2) and Si70Ge30
alloy nanowire devices; both devices were annealed using
RTA at 400 ◦C for 30 s in a nitrogen atmosphere. It is clear
that devices with Ni/Au contacts show resistance switching
behavior regardless of the Ge content. Highly nonlinear
I–V characteristics were observed from a Ni/Au-contacted Si70Ge30
alloy nanowire device, with non-zero current at zero bias. We
suspect that such a behavior is originated from the deformed
contact shown in the TEM image of figure 4, which could
behave as a charge trap.

From the TEM analysis, we identified enhanced Au layers
at the contact front of Ni/Au-contacted Si1−xGex nanowire
devices. As a control experiment, we also fabricated Si1−xGex
alloy nanowire devices on a transparent membrane with only
Ni contact electrodes. The inset in figure 3(b) shows the I–V
characteristics of a Ni-contacted Si70Ge30 alloy nanowire
device at different source–drain bias voltages (red curve at
Vsd = 1 V, blue 3 V, green 5 V, and black 7 V). Devices
with only Ni contact electrodes did not show the resistance
switching effect seen in the case of Ni/Au-contacted ones.
Although they showed relatively high resistance compared
with Ni/Au-contacted devices, clear p-type gate responses
were also observed in the Ni contact devices (data not shown).
Figure 2. TEM images and EDS analysis of a Ni/Au-contacted Si_{95}Ge_{5} alloy nanowire device. (a) TEM images of the nanowire device; scale bar 10 µm. The inset shows a magnified view of this particular device; scale bar 1 µm. (b) HRTEM image of the device (arrows point to sites of EDS analysis), and (c) relative atomic percentage of the constituents at different positions. The left-most arrow in (b) is position 1, and the red arrow corresponds to position 3.

The observed hysteresis in the $I$–$V$ curves could be the result of surface defects or a contact effect rather than the presence of gold in the wire near the contacts. We also suspect that surface effects may influence in part the observed hysteric behavior. However, the hysteretic behavior due to the surface charge carrier trapping in the channel has been normally observed in the gate response curve, not in the $I$–$V$ curve. We could also observe similar hysteretic $I$–$V$ curves even in a high vacuum condition after an extensive pumping process. Thus, we think that the major effect of the hysteretic gate response could originate from the gold buried near the contact region. We believe that this can be an indirect proof that the observed hysteresis could be unrelated to the surface traps.

HRTEM images and EDS analysis of Ni-contacted Si_{70}Ge_{30} alloy nanowire devices are shown in the supporting information figure S6 (available at stacks.iop.org/Nano/20/115708). No Au atoms were found along the length of a Ni-contacted Si_{70}Ge_{30} alloy nanowire, and the channel length is much longer than that of the Ni/Au-contacted channels. In the case of Ni/Au contacts, a Si_{95}Ge_{5} alloy nanowire device with an original channel length of 1.5 µm shrank to 200 nm after annealing, and a Si_{70}Ge_{30} alloy nanowire device with a 2 µm channel length shrank to 400 nm; however, the channel length of a Ni-contacted Si_{70}Ge_{30} alloy nanowire device changed from approximately 2 to 1 µm. Both nanowires have approximately the same diameter of ~100 nm. Since the activation energy barrier for diffusion of Au in Si (1.12 eV) is lower than that of Ni (1.9 eV) [21], Au penetrates much more quickly than Ni, forming a shorter channel. In bulk Si_{60}Ge_{40} films annealed at 400°C, Au-mediated diffusion occurs with a velocity of 19 nm s$^{-1}$, while Ni-mediated alloys formed at ~4.2 nm s$^{-1}$ [22]. In our case, diffusion mediated by Ni/Au in the Si_{70}Ge_{30} alloy nanowire occurred at ~27 nm s$^{-1}$, and that mediated by Ni occurred at ~16 nm s$^{-1}$. These values are slightly higher than those in bulk films, but the diffusion depth of metal decreases with increasing Ge concentration [22], and we might expect axial diffusion only, in the case of one-dimensional nanostructures. We also expect lower electrical conductance from Ni-contacted alloy nanowire devices because the conductance is inversely proportional to the channel lengths in diffusive systems. The effect of the
channel length is insufficient to explain the observed two-orders-of-magnitude decrease in conductance measured from the Ni-contacted alloy nanowire device. Recently, Nam et al [23] and Tham et al [24] reported low resistance ohmic contacts on GaN nanowires with focused ion beam (FIB) deposited electrode, and explained it by the presence of amorphous GaN under the contact using cross-sectional TEM analysis. We cannot completely rule out the possibility of Au doping by further diffusion of Au atoms into the nanowire during the annealing process, as it is known that a very small amount of Au atoms from an Au catalyst can migrate along the nanowire surface during VLS growth [12, 13]. Or, since AuSi is expected to have a comparable work function to that of PtSi (4.97 eV), the Schottky barrier height with the valence band of SiGe would be lower than in the case of NiSi contacts (4.7 eV) [25].

We also performed HRTEM and EDS analyses of Ni/Au-contacted Si_{70}Ge_{30} alloy nanowire devices (figure 4). As in the case of the Si_{95}Ge_{5} alloy nanowire device, we found Au-rich regions at the contact front, and one of the contacts showed severe deformation. EDS analysis (supporting information figure S7 (available at stacks.iop.org/Nano/20/115708)) revealed an abrupt decrease in Ge content at the contact front, where Au forms an alloy with the nanowire. As mentioned previously, we also observed a nonlinear transport characteristic in this particular device (figure 3(b)); the observed contact deformation may explain this behavior.

Missing Ge at the contact front does not only occur with Ni/Au-contacted devices: we observed similar behavior with Ni-contacted alloy nanowire devices. Figure 5 shows EDS maps of a Ni-contacted Si_{70}Ge_{30} alloy nanowire device. Even in this case, Ge disappears abruptly at the contact front, though it is still observed in nickel germanosilicide regions. Because the formation energies of NiSi and NiGe are $\Delta H_{\text{NiSi}} = -45$ and $\Delta H_{\text{NiGe}} = -32 \text{ kJ mol}^{-1}$, respectively [26], Ni will prefer to react with Si rather than Ge. According to the observations reported by Pey et al [27], Ge diffuses out of nickel germanosilicide and Si moves in, thereby increasing the Si content in nickel germanosilicide. The Ge that diffuses out tends to form Ge-rich Si$_{1-z}$Ge$_z$ grains, where $z > x$. Therefore, we may expect to encounter decreased Ge content at the contact front where the formation of Ni silicide is most intense.

4. Summary

We have shown that alloy nanowire devices with Ni/Au contacts annealed with RTA show resistance switching behavior, and that such behavior strongly depends on the diffusion of Au atoms. It is not currently known how diffused Au atoms can contribute to the observed anomalous resistance switching behavior. As silicon-rich AuSi is a semiconductor,
Figure 5. EDS maps of a Ni-contacted Si$_{70}$Ge$_{30}$ alloy nanowire device annealed at 400 °C. The absence of the Ge K signal is apparent at the contact region.

it may store charge for some time; however, more extensive analysis of the AuSi at the contact front is necessary to resolve this phenomenon. A microscopic interface between a metal and a semiconductor nanostructure is indeed crucial for the electrical properties of devices, and exploiting such interface sensitivity may provide a basis for new device concepts.

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